



Unigraf DisplayPort™ CTS Tools



Guide to Product Options



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GENERAL

Reference Standards

VESA® DisplayPort® Link Layer Compliance Test Specification
Version 1.2 Core Revision 1.1 December 8, 2012

VESA® DisplayPort® Link Layer Compliance Test Specification:
Extension Set 1, Rev 1.1, December 28, 2012

HDCP Specification v1.3; Amendment for DisplayPort rev 1.1,
15 Jan 2010

Release Version

This document explains features found in the following versions of the software:

Tool	Version	Issued
Unigraf DP Reference Source CTS	3.3.0	26.03.2013
Unigraf DP Reference Sink CTS	3.3.2	07.03.2013
Unigraf DP LL CTS Extensions, Set A	1.21	20.05.2013

DP REFSINK CTS TOOLS

DP Reference Sink Products

Product	P/N	Description
DPR-100	065910	Compact sized DP Reference Sink with DP Sink Console software
UFG-04 DP-512	062745	DP Reference Sink and frame grabber with DP Sink Console software

CTS Test Product Options for Reference Sinks

Product	P/N	Tests included
DP RefSink CTS LL	065033	- Link Layer CTS for testing Transmitters
DP RefSink CTS LL & HDCP	065037	- Link Layer CTS for testing Transmitters - HDCP CTS for Testing Transmitters
DP RefSink CTS LL & HDCP & EXT HDCP	065038	- Link Layer CTS for testing Transmitters - HDCP CTS for Testing Transmitters - Extended HDCP CTS for testing Transmitters and Repeaters
DP RefSink Audio CTS	065043	- Audio CTS for Testing Transmitters

Description of CTS Tests for Reference Sinks

Link Layer CTS for testing Transmitter DUT

Test Reference	Test Name
(4.2.1.1)	Source DUT Retry on No-Reply During Aux Read after Hot Plug Event
(4.2.1.2)	Source Retry on Invalid Reply During Aux Read after Hot Plug Event
(4.2.2.1)	EDID Read upon Hot Plug Event
(4.2.2.2)	DPCD Receiver Capability Read upon Hot Plug Event
(4.2.2.3)	EDID Read
(4.2.2.4)	EDID Read failure #1: I2C-Over-AUX NACK
(4.2.2.5)	EDID Read failure #2: I2C-Over-AUX DEFER
(4.2.2.6)	EDID Corruption Detection
(4.2.2.7)	Branch Device Detection upon HPD Plug Event

Link Layer CTS for testing Transmitter DUT (cont.d)

(4.2.2.8)	EDID read on IRQ_HPDP event after Branch Device detection
(4.2.2.9)	E-DDC Four Block EDID Read
(4.3.1.1)	Successful Link Training Upon HPDP Plug Event
(4.3.1.2)	Successful Link Training at All Supported Lane Counts and Link Speeds
(4.3.1.3)	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence
(4.3.1.4)	Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing
(4.3.1.5)	Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing
(4.3.1.6)	Successful Link Training with Request of a Higher Pre-emphasis Setting During Channel Equalization Sequence
(4.3.1.7)	Successful Link Training at Lower Link Rate due to Loss of Symbol Lock During Channel Equalization Sequence
(4.3.1.8)	Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing
(4.3.1.9)	Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing
(4.3.1.10)	Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5)
(4.3.2.1)	Successful Link Re-training After IRQ HPDP Pulse Due to Loss of Symbol Lock
(4.3.2.2)	Successful Link Re-training After IRQ HPDP Pulse Due to Loss of Clock Recovery Lock
(4.3.2.3)	Successful Link Re-training After IRQ HPDP Pulse Due to Loss of Inter-lane Alignment Lock
(4.3.2.4)	Handling of IRQ HPDP Pulse With No Error Status Bits Set
(4.3.2.5)	Lane Count Reduction
(4.3.2.6)	Lane Count Increase
(4.3.3.1)	Video Time Stamp Generation
(4.4.1.1)	Pixel Data Packing and Steering
(4.4.1.2)	Main Stream Data Packing and Stuffing – Least Packed TU
(4.4.1.3)	Main Stream Data Packing and Stuffing – Most Packed TU
(4.4.2)	Main Video Stream Format Change Handling
(4.4.3)	Power Management
(700.1.1.1)	Additional DPCD Handling Test 1
(700.1.1.2)	Additional DPCD Handling Test 2

HDCP CTS for Testing Transmitter DUT

Test Reference	Test Name
(1A-01)	Regular Procedure: With Receiver
(1A-02)	Regular Procedure: HPD After Writing Aksv
(1A-03)	Regular Procedure: HPD During Link Integrity Check Stage
(1A-04)	Irregular Procedure: (First Part of Authentication) Failure to Read Bcaps HDCP_CAPABLE Bit
(1A-05)	Irregular Procedure: (First Part of Authentication) Verify Bksv
(1A-06)	Irregular Procedure: (First Part of Authentication) Verify R0'
(1A-07)	Irregular Procedure: (Link Integrity Check) Link Integrity Failure
(1A-08)	Irregular Procedure: SRM
(1A-09)	Regular Procedure: Encryption Disable Bootstrapping

Extended HDCP CTS for Testing Transmitter and Repeater DUT

Tests for Transmitter DUT:

Test Reference	Test Name
(1B-01)	Regular Procedure: With Repeater
(1B-02)	Irregular Procedure: Spurious CP_IRQ Interrupt
(1B-03)	Regular Procedure: HPD after Reading R0'
(1B-04)	Irregular Procedure: (Second part of Authentication) Timeout of KSV List READY
(1B-05)	Irregular Procedure: (Second part of Authentication) Verify V'
(1B-06)	Irregular Procedure: (Second part of Authentication) MAX_DEVS_EXCEEDED
(1B-07)	Irregular Procedure: (Second part of Authentication) MAX_CASCADE_EXCEEDED

Tests for Repeater DUT:

Test Reference	Test Name
(3A-01)	Regular Procedure: With Receiver
(3A-02)	Irregular Procedure: (First part of Authentication) Failure to Read Bcaps HDCP_CAPABLE Bit
(3A-03)	Irregular Procedure: (First part of Authentication) Verify Bksv
(3A-04)	Irregular Procedure: (First part of Authentication) Verify R0'
(3B-01)	Regular Procedure: With Repeater
(3B-02)	Irregular Procedure: (Second part of Authentication) Timeout of KSV List READY

**Extended HDCP CTS for Testing Transmitter and Repeater DUT
Tests for Repeaters (cont.d)**

(3B-03)	Irregular Procedure: (Second part of Authentication) Verify V'
(3B-04)	Irregular Procedure: (Second part of Authentication) MAX_DEVS_EXCEEDED
(3B-05)	Irregular Procedure: (Second part of Authentication) MAX_CASCADE_EXCEEDED

Audio CTS for Testing Transmitter DUT

Test Reference	Test Name
(4.4.4.2)	Audio Stream Header Synchronization
(4.4.4.3)	Audio Time Stamp Generation
(4.4.4.4)	Audio InfoFrame Packet
(4.4.4.5)	Audio Stream Transmission
(4.4.4.6)	Audio Start Sequence

DP REFSOURCE CTS TOOLS

Reference Source Products

Product	P/N	Description
DPT-200	065921	Compact sized DP Reference Source with DP Source Console software
VTG-5225 DP	065031	DP Reference Source and Pattern Generator with WinVTG GUI software

CTS Test Product Options for Reference Sources

Product	P/N	Tests included
DP RefSource CTS LL	065032	- Link Layer CTS for testing Receivers
DP RefSource CTS LL & HDCP	065036	- Link Layer CTS for testing Receivers - HDCP CTS for Testing Receivers
DP RefSource CTS LL & HDCP & EXT HDCP	065045	- Link Layer CTS for testing Receivers - HDCP CTS for Testing Receivers - Extended HDCP CTS for Testing Repeaters

Description of CTS Tests for Reference Sources

Link Layer CTS for testing Receiver DUT

Test Reference	Test Name
(5.2.1.1)	Read One Byte from Valid DPCD Address
(5.2.1.2)	DPCD Receiver Capability Read (Read Twelve Bytes from Valid DPCD Address)
(5.2.1.3)	Write One Byte to Valid DPCD Address
(5.2.1.4)	Write Nine Bytes to Valid DPCD Addresses
(5.2.1.5)	Write EDID Offset (One Byte I2C-Over-Aux Write)
(5.2.1.6)	Read One EDID Byte (One Byte I2C-Over-Aux Read)
(5.2.1.7)	EDID Read (1 Byte I2C-Over-Aux Segment Write, 1 Byte I2C-Over-Aux Offset Write, 128 Byte I2C-Over-Aux Read)
(5.2.1.8)	Illegal Aux Request Syntax
(5.2.1.9)	Glitch Rejection

Link Layer CTS for testing Receiver DUT (cont.d)

(5.2.1.10)	Interleaved EDID and DPCD Receiver Capability Read
(5.2.1.11)	Downstream Stop on MOT Reset
(5.2.1.12)	Downstream Stop on MOT Timeout
(5.3.1.1)	Successful Link Training at All Supported Lane Counts and Link Speeds
(5.3.1.2)	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence
(5.3.1.3)	Successful Link Training to a Lower Link Rate Due To Clock Recovery Lock Failure During Clock Recovery Sequence
(5.3.1.4)	Successful Link Training with Request of a Change to Pre-Emphasis and/or Voltage Swing Setting During Channel Equalization Sequence
(5.3.1.5)	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence
(5.3.1.6)	Lane Count Reduction
(5.3.1.7)	Lane Count Increase
(5.3.2.1)	IRQ_HPDPulse Due to Loss of Symbol Lock and Clock Recovery Lock
(5.3.2.2)	IRQ HPDPulse Due to Loss of Inter-lane Alignment Lock
(5.4.1.1)	Pixel Data Reconstruction
(5.4.1.2)	Main Stream Data Unpacking and Unstuffing – Least Packed TU
(5.4.1.3)	Main Stream Data Unpacking and Unstuffing – Most Packed TU
(5.4.1.4)	Pixel Clock Recovery (<i>Note: Informative, HW does not support SSC</i>)
(5.4.2)	Main Video Stream Format Change Handling
(5.4.3.1)	Entering and Exiting Power Save Mode
(5.4.3.2)	Resumption of Main Link Activity After Extended Idle
(7.2.1.1)	Sink Organizationally Unique Identifier (OUI)
(7.2.1.2)	Sink Count
(7.2.1.3)	Sink Status
(7.2.1.4)	Symbol Error Count
(7.2.1.5)	Device Identifications
(7.2.1.6)	Number of Receiver Ports
(7.2.1.7)	Main Link Channel Coding

HDCP CTS for Testing Receiver DUT

Test Reference	Test Name
(2A-01)	Regular Procedure: With Transmitter
(2A-02)	Irregular Procedure: (First Part of Authentication) New Authentication
(2A-03)	Irregular Procedure: (Link Integrity Check) New Authentication
(2A-04)	Regular Procedure: Encryption Disable Bootstrapping

Extended HDCP CTS for Testing Repeater DUT

Test Reference	Test Name
(3C-01)	Regular Procedure: Transmitter - DUT - Receiver
(3C-02)	Regular Procedure: HPD Propagation when an Active Receiver is Disconnected and Reconnected Downstream
(3C-03)	Regular Procedure: HPD Propagation when an Active Receiver is Disconnected Downstream
(3C-04)	Regular Procedure: HPD Propagation when an Active Receiver is Connected Downstream
(3C-05)	Irregular Procedure: (First part of Authentication) New Authentication
(3C-06)	Irregular Procedure: (Second part of Authentication) New Authentication
(3C-07)	Irregular Procedure: (Link Integrity Check) New Authentication
(3C-08)	Irregular Procedure: (Second part of Authentication) Verify Bksv
(3C-09)	Irregular Procedure: (Second part of Authentication) Verify R0'
(3C-10)	Regular Procedure: Transmitter - DUT - Repeater
(3C-11)	Regular Procedure: HPD After Writing Aksv
(3C-12)	Regular Procedure: HPD After Reading R0'
(3C-13)	Regular Procedure: HPD After Starting Third part of Authentication
(3C-14)	Irregular Procedure: (Second part of Authentication) Verify V'
(3C-15)	Irregular Procedure: (Second part of Authentication) DEVICE_COUNT
(3C-16)	Irregular Procedure: (Second part of Authentication) DEPTH
(3C-17)	Irregular Procedure: (Second part of Authentication) MAX_DEVS_EXCEEDED
(3C-18)	Irregular Procedure: (Second part of Authentication) MAX_CASCADE_EXCEEDED

Audio CTS for Testing Receiver DUT

Currently not available

DP 1.2 LL CTS EXTENSIONS

DP Reference Sink Products

Product	P/N	Description
DPR-120	065912	HBR2 and MST compliant Reference Sink

CTS Test Product Options for Reference Sinks

Product	P/N	Tests included
Unigraf DP LL CTS Extensions, Set A	065913	- A limited set containing of link training related tests from DP LL CTS Extensions1 (pls see list below)

Description of CTS Tests for DPR-120

Link Layer Extension Test Set A for Testing Transmitter DUT

Test Reference	Test Name
(400.3.1.1)	Successful Link Training at All Supported Lane Counts and Link Speeds: HBR2 Extension
(400.3.1.2)	Successful Link Training with Request of Higher Differential Voltage Swing During Clock Recovery Sequence: HBR2 Extension
(400.3.1.3)	Successful Link Training to a Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension
(400.3.1.4)	Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension
(400.3.1.5)	Successful Link Training with Request of a Higher Pre-emphasis and Post Cursor 2 Setting During Channel Equalization Sequence
(400.3.1.6)	Successful Link Training at Lower Link Rate Due to Loss of Symbol Lock During Channel Equalization Sequence: HBR2 Extension
(400.3.1.7)	Unsuccessful Link Training at Lower Link Rate #1: Iterate at Max Voltage Swing: HBR2 Extension
(400.3.1.8)	Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing: HBR2 Extension
(400.3.1.9)	Unsuccessful Link Training due to Failure in Channel Equalization Sequence (loop count > 5): HBR2 Extension
(700.1.1.1)	Additional DPCD Handling Test 1
(700.1.1.2)	Additional DPCD Handling Test 2